VLSI 1

Lab 3A Report: Design Summary

*Transmit*

For the transmit side the design flow goes from 8 bit input, to 4 byte FIFO, to 8 bit shift register, to serial output. If we receive additional 8 bit inputs while processing the first, we simply queue these in the FIFO. Once the output shift register is loaded with the 8 bit input from the FIFO, we shift out one bit at a time for 8 clock cycles. One clock cycle before the first bit we also assert the SSPFSS pin.

*Receive*

For the receive side we tried to reverse the information flow of the transmit side. Once we receive an SSPFSS signal, we shift in bits to a shift register from the serial data pin. After 8 clock cycles we have a valid byte, so we assert a valid data signal to the fifo. We then load the 8 bit value into the next available spot in the FIFO. If it is full, we ignore the incoming data. When the processor asserts the PSEL and deasserts the PWRITE pins, we load the data from the first address of the FIFO to the output pins to the processor.